A CONTROL STRATEGY BY INSTANTANEOUS AVERAGE VALUES FOR PARALLEL OPERATION OF SINGLE PHASE VOLTAGE SOURCE INVERTERS BASED IN THE INDUCTOR CURRENT FEEDBACK

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Abstract - This paper presents a simple, effective and robust control strategy applied to parallel connected of single phase voltage source inverters. The parallelism control is only done using internal measures of each inverter. The objective is to obtain a control system where the inverters are independent from each other. The proposed control strategy of each inverter has two control loops by instantaneous average values: one for voltage and another for current. The first one is designed to control the output voltage of the inverter, while the second is designed to lead the parallel operation of the inverters. The parallelism control acts in the voltage before the LC filter and it is based on the feedback of the L inductor current. Its function is to guarantee the correct load current sharing. The control technique was corroborated through experimental results with a maximum load of 10 kVA supplied by three parallel connected inverters.

Index Terms - Control strategy, parallelism, single phase, voltage source inverters.

I. INTRODUCTION

Usually, the parallel configuration of VSI (voltage source inverters) is applied to share the processed load power, to obtain redundancy, to improve the reliability and to make flexible the power expansion. A redundant and modular system must have inverters that are completely independent and without any communication among them, in order to the system works suitably.

Some applications of parallel inverters are UPS [1]–[22] and, more recently, connecting renewable power sources in an isolated distributed generation network [23]–[27].

When voltage source inverters are connected in parallel, small deviations in the output voltage of each module can generate current circulation and disequilibrium in the power processed by them. There are situations, especially in non-load operation, that an inverter becomes a load to the others, consuming active and reactive power. Those deviations are inherent to the system on account of the components differences and numeric errors of digital control processors. This is a very sensible structure on the grounds that it connects voltage sources in parallel.

In the literature there is no standard solution for this application. There are many publications based on the following techniques: master-slave [1]–[3], central mode control [4]–[5], distributed logic control [6]–[11] and wireless control (or frequency and voltage droop) [12]–[27]. The master-slave and central mode control techniques present an effective current sharing control, but they do not allow a true redundancy because a failure in the master or in the central unit would shutdown the whole system. The distributed logic control may be implemented based on current control or power deviation control [10]. Each inverter has its own control system for the parallel operation, improving the redundancy and modularity of the system in comparison to the two previous techniques. This scheme has a communication bus which all units connected to the system share data to ensure the proper operation. Failures in the data bus will also shutdown the system. The strategy that gives a true redundancy, in which the inverters are completely independent of each other, is the wireless control. It is based on the frequency and voltage droop principles of power systems and the control is done by power average values. This strategy is difficult to implement due to the calculation of the average powers. Furthermore, it has a slow dynamic response and admits a bigger error in the distribution of power between the inverters than the previous techniques. Studies of [16]–[22] demonstrate strategies to minimize these disadvantages.

Taking these facts into account, this paper presents a control strategy for parallel operation of single phase voltage source inverters. This strategy can be classified how wireless control, because the inverters are independent of each other and they are not communication among them.

II. CONCEPTION OF THE CONTROL STRATEGY

This paper is proposing a control strategy for parallel connected single phase voltage source inverters. Fig 1 shows the broached structure, in which each VSI is called of module. In module 1 is presented the complete structure with power and control circuits of one voltage source inverter. The other modules are identical to the module 1 and they are illustrated as a block in Fig 1. As inverters are independent of each other, all the study of the proposed control strategy can be done analyzing the behavior of only one inverter.
Each inverter has its own control circuit, as shown in module 1 from Fig 1. The proposed strategy has two control loops by instantaneous average values [28] in each inverter, as shown in module 1. The first loop controls the output voltage of the inverter ($V_0$). The main advantages of the $V_0$ control by instantaneous average values are the good static regulation and the low THD of the output voltage, even when non-linear loads are supplied. This control loop has a voltage reference ($V_{ref}$) that must be synchronized with the voltage references of the other modules. This can be done through a PLL (phase locked loop) that, using a reference signal derived from electrical utility system, can synchronize the voltage references. With all synchronized reference voltages, if the electrical utility system fails, the PLL sustains the synchronism for a time interval. If the system autonomy of parallel inverters is larger than this time interval, during the failure the PLL can use the own $V_0$ voltage to sustain the synchronism of the reference voltage. The second loop is responsible for the parallelism control. Its aim is to guarantee the correct load current sharing among the inverters. The technique is based on control by instantaneous average values of the voltage from the inverter before the LC filter ($V_{AB}$). This control is performed through the feedback of the current $I_L$ and it is placed in cascade with the voltage controller in order to actuate in the $V_{AB}$ voltage. Regarding the fact that the modules do not communicate with each other, details from the load and other inverters currents can not be obtained, so, there is no information to calculate a reference value for $I_L$.

In the inverter control system, shown in module 1 from Fig 1, the voltage loop obeys the control law of (1).

$$V_{cv}(t) = (V_{ref}(t) - V_0(t) \cdot K_v) \cdot C_v$$

(1)

The voltage error signal ($e$) is applied in the voltage controller $C_v$. The compensated error signal ($V_{cv}$) from the voltage loop is the point of action for the parallelism control. This control consists in subtract $V_{cv}$, which is proportional to inductor $L$ current, to the signal $V_{cp}$. The output signal of the parallelism control ($V_{cp}$) is defined in (2).

$$V_{cp}(t) = V_{cv}(t) - I_L(t) \cdot K_{IL}$$

(2)

The $V_{cp}$ signal is applied in the PWM modulator that generates the $V_{AB}$ voltage, as defined in (3).

$$V_{AB}(t) = K_{inv} \cdot V_{cp}(t)$$

(3)
The static gain of the inverter and the PWM modulator are represented by \( K_{\text{inv}} \) which are defined in (4). The \( V_{cc} \) is the DC link voltage, \( n \) is the transformer relation and \( V_p \) is the peak value of PWM carrier.

\[
K_{\text{inv}} = \frac{V_{cc} \cdot n}{V_p}
\]  
(4)

The proposed parallelism control grounds in a proportional controller \( (K_{IL}) \), placed on the \( I_L \) current feedback. Thus, the signal of the current feedback loop \( (V_I) \) acts instantly in \( V_{cv} \) and, as a consequence, it acts instantly in the \( V_{AB} \) voltage, providing a fast dynamic response to current variations. The \( K_{IL} \) gain quantifies the control action of (2). The current feedback also works as an overcurrent protection for the inverter.

Using (2) and (5) in (3), (6) is obtained.

\[
V_{AB}(t) = K_{IL} \cdot I_l \cdot K_{IL}
\]  
(5)

\[
V_{AB}(t) = K_{IL} \cdot V_{cv}(t) - K_{IL} \cdot I_l(t)
\]  
(6)

Defining \( K_I \) gain in (7) and \( V_{AB0} \) in (8). The \( V_{AB0} \) represents the \( V_{AB} \) voltage without the action of the current feedback loop.

\[
K_I = K_{IL} \cdot K_{IL}
\]  
(7)

\[
V_{AB0}(t) = K_{IL} \cdot V_{cv}(t)
\]  
(8)

Replacing (5), (7) and (8) in (6), is found (9).

\[
V_{AB}(t) = V_{AB0}(t) - K_I \cdot I_l(t)
\]  
(9)

The analysis of (9) proves that instantaneous variations of \( I_L \) cause instantaneous variations in \( V_{AB} \). The parallelism control law presents the instantaneous droop curves characteristics, reducing the \( V_{AB} \) voltage due the increase of \( I_L \) according to (9).

The parallelism control based on the feedback of \( I_L \) current acts modifying the inverter \( V_{AB} \) voltage. In this strategy the parallelism control does not change the reference voltage and keep the output voltage \( V_o \) imposed only by the voltage loop. These characteristics assure that \( V_o \) voltage of all inverters remain synchronized with their voltage references and, as a consequence, synchronized among them.

III. ANALYTICAL STUDY OF THE CONTROL STRATEGY IN A SINGLE INVERTER

A. Small Signal Model

Fig 2 shows the block diagram of the voltage and the current feedback loops for one inverter. As both loops have similar dynamic responses, it is not possible to uncouple them. So, the small signal model of the inverter, which is used in the voltage loop design, must take into account the \( I_L \) inductor current feedback.

The small signal model of the inverter for \( I_L \) derivative from \( V_{cp} \) signal, defined as \( G_I(s) \), is shown in (10). The C is the LC filter capacitance, L is the LC filter inductance and \( Z_o \) is the load impedance. The \( K_{IL} \) controller is designed to satisfy the inverters parallel operation specification. The closed loop transfer function of the current loop, \( I_{CLTF}(s) \), is shown in Fig 2 and is considered without simplifications in the model of the inverter for the voltage loop.

The transfer function \( G_v(s) \) of \( V_o \) in function of \( I_L \) is defined in (11). The small signal model of the inverter for \( V_o \) derive from the control signal \( V_{cv} \) is represented by the open loop transfer function (OLTF) \( G_v(s) \), defined in (12). Knowing \( G_v(s) \), it is possible to choose and design \( C_v(s) \). The selected voltage controller \( C_v(s) \) was the PID and it is defined in (13). The blocks diagram of Fig 2 shows with details how all the transfer functions are related.

\[
I_L(s) = G_I(s) = \frac{s \cdot C + \frac{1}{Z_o}}{s^2 \cdot L \cdot C + s + \frac{L}{Z_o} + 1}
\]  
(10)

\[
V_o(s) = G_v(s) = \frac{1}{s^2 \cdot C + s + \frac{1}{Z_o} \cdot K_{IL} \cdot K_{inv}}
\]  
(11)

\[
\frac{V_o(s)}{V_{cv}(s)} = G_{v2}(s) = \frac{K_{inv}}{s^2 \cdot L \cdot C + s + \frac{L}{Z_o} + K_{IL} \cdot C \cdot K_{inv}} + \left[ 1 + \frac{K_{IL} \cdot K_{inv}}{Z_o} \right]
\]  
(12)

\[
C_v(s) = K_{cv} \cdot \frac{(s + z_1)(s + z_2)}{(s + p_1)}
\]  
(13)

B. Study of the Inductor Current Feedback in the Voltage Source Inverter

Equation (12) shows that the feedback of the inductor \( L \) current changes the position of the poles of the voltage loop transfer function as the \( K_{IL} \) gain value. So, the adjustment of the current feedback loop gain changes the static and dynamics characteristics of the voltage inverter. This can be verified in the equations of the static gain \( K_{G2} \) and the damping \( \xi_{G2} \) of \( G_{G2} \), shown in (14) and (15). In these expressions \( Z_o \) is replaced by a resistive load \( R_p \).

Equation (14) shows that the current feedback reduces the static gain of the inverter, when \( K_{IL} \) gain increases. Moreover, the equation (14) shows that the static gain decreases in proportion with the load increasement \( (R_p) \) load reduction). Therefore, in non-load the static gain is equal to \( K_{inv} \), in other words, without the influence of the \( I_L \) current feedback.

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Equation (15) shows that the current feedback also changes the dynamic response of the inverter, more specifically, the damping. In this case, the inductor current feedback adds a term to the damping equation, which does not depend on the $R_o$ load. This term is proportional to $K_{IL}$ gain and the $C$ capacitor. This characteristic assures the increase of the inverter damping, even in non-load operation.

The effect of the $I_L$ current feedback can be seen in the simulations presented in Fig 3 and Fig 4. Both figures present the behavior of $V_o$ for one inverter. They were obtained with the transfer function of (12) applying a unitary step in $V_{cv}$. The parameters are used to draw the figures which are shown in section IV.

![Image](image-url)

**Fig 3.** $V_o$ voltage in one inverter for low load simulation with and without $I_L$ current feedback loop.

![Image](image-url)

**Fig 4.** $V_o$ voltage in one inverter for nominal load simulation with and without $I_L$ current feedback loop.

![Image](image-url)

**Fig 5.** Bode magnitude diagrams for one inverter with loads and $K_{IL}$ values different.

Fig 3 shows a low load situation ($R_o=100 \, \Omega$). In this simulation the dynamic and static responses of the inverter with ($K_{IL}=0.01$) and without ($K_{IL}=0$) current feedback is compared. The result obtained with the current feedback loop have lower overshoot, settling time and oscillations, and it achieves the steady-state faster, that are typical characteristics of damping increase. However, the $V_o$ values in steady-state of both simulations were similar.

Fig 4 presents the simulation under nominal load ($R_o=10 \, \Omega$), and, again, it is compared the dynamic and static response of the inverter with ($K_{IL}=0.01$) and without ($K_{IL}=0$) the current feedback loop. The transitory responses show that case with current feedback has again an overshoot and setting times fewer than the case without current feedback. As the load gets higher, an interesting particularity in steady-state can be seen, the case with current feedback loop presents a lower value of $V_o$ than the case where the current feedback loop is not present, due to inverter static gain drop, as shown in (14).

Plotting the Bode diagrams of the transfer function of (12) for the same conditions presented in Fig 3 and Fig 4, is found the results of magnitude, Fig 5, and phase, Fig 6. In these diagrams the curves A and B were simulated with $K_{IL} = 0$ (without current feedback) under low load and nominal load, respectively. The curves C and D were simulated with $K_{IL} = 0.01$ (with current feedback) and they also present the results under low load and nominal load, respectively.

Analyzing the curves A and C of Fig 5, cases of low load, the inductor current feedback loop reduces the inverter gain in the resonance frequency area. The curves B and D of the Fig 5 show that, under nominal load, the inverter with the inductor current feedback presents an improvement in the damping in the resonance frequency and, besides that, there is a decrease in the gain to low frequencies.
The curves in Fig 6 show that the presence of the current feedback changes the phase diagram, which can improve the phase margin of the inverter and, as a consequence, its stability.

The characteristics introduced to the VSI with the \( I_L \) current feedback loop will be very important to the parallelism control. The inverter damping increase allows the parallel connection of inverters in any level of load, with smooth transitory in the voltage output. The decrease of the static gain in proportion to the increase of the supplied load assures the correct load sharing among the inverters. In a situation with two or more inverters connected in parallel, if there is a current disequilibrium among them, the inverter that supplies the greatest current will have a greater reduce in its static gain and, as a consequence, the current supplied by this inverter will be decreased. Then, the system achieves a working point according to the \( K_{IL} \) gain, that can be the adequate current load sharing among the inverters. Besides that, a correct adjustment of the \( K_{IL} \) gain also allows to connect inverters with different power levels in parallel, assuring that each one supplies to the load the current in proportion to their nominal power. Another relevant fact is that the instantaneous inductors current feedback loop ensures a fast dynamic response, which is necessary to the parallelism control of VSI. All these characteristics obtained with the inductor current feedback loop together allowed the use of this control in the parallelism of voltage source inverters.

C. Understanding the Inductor Current Feedback Loop as a Virtual Impedance

The inverter 1 from Fig 1 (module 1) can be represented through simplified equivalent circuit of Fig 7, where the Full Bridge inverter and the PWM modulator are simplified by a controlled voltage source, which it obeys (3). This simplification does not take into account the high frequency from \( V_{AB} \) voltage of the inverter. The \( Z_{out} \) impedance represents the \( C \) capacitor and the \( Z_{load} \).

Using (7) in (9) is gotten (16). This expression shows that \( V_{AB} \) voltage is composed of two parts: the first \( (V_{AB0}) \) is consequence from the voltage control; and the second \( (KI_L) \) is from the feedback current. The result of this second part is a voltage droop proportional to \( K_I \) gain, which can be interpreted as an impedance. So, it is possible to express the action of the feedback of the \( L \) inductor current in the inverter control by a virtual impedance in the power circuit, how it is shown in Fig 8. In this figure, the \( V_{AB0} \) voltage source (define in (8)) is controlled by signal \( V_{cv} \), because this voltage represents the part of \( V_{AB} \) voltage due to the voltage control. The \( K_I \) virtual impedance, define in (7), is just a gain and therefore, this impedance has resistive characteristics. The transfer function of the circuit shown in Fig 8 is equal to the transfer function of (12), confirming the analogy. The conception of virtual impedance in the control of parallel inverter is presented in [16]–[17].

\[
V_{AB}(t) = V_{AB0}(t) - K_I \cdot I_L(t) \quad (16)
\]

The understanding of the parallel control as a virtual impedance in series with \( L \) inductor, as shown in Fig 8, denotes one of the principles of this strategy that is to control the parallel operation of VSI acting in the voltage before the LC filter, called \( V_{AB} \). Thus, the output voltage \( V_o \) is only imposed by voltage loop. The virtual impedance \( K_I \) is not a connection impedance between the inverter and common ac bus, because it is placed before LC filter. This fact keeps the controlled voltage \( V_o \) connected the load.

IV. IMPLEMENTATION AND EXPERIMENTAL RESULTS

Two prototypes were implemented to corroborate the control strategy. One with three inverters of 5 kVA connected in parallel and another prototype with two inverters of 5 kVA and one of 2.5 kVA connected in parallel.
Each module has an AC-DC converter powered by the electric utility system, a DC-AC inverter, a transformer, an LC filter and the proposed control system. The voltage of the electric utility system and the output voltage of the inverters are 220 V RMS, with a frequency of 60 Hz. In the inverter control system, analog circuits were used. The PWM modulator was digitally implemented using a PIC18F2331 microcontroller. For the power circuit (AC-DC and DC-AC) one Semikron module 50B6U+SKS B2C110V6 was used. The main project values of 5 kVA inverters were: $L=1100 \mu H$, $C=36 \mu F$, $n=1.63$, $K_{IL}=0.015 \Omega$, $z_1=888$ Hz, $z_2=328$ Hz, $\rho_1=34050$ Hz, $K_{CV}=14.7$, $K_c=0.016$ and a switching frequency of 10 kHz. The main project values of 2.5 kVA inverter were: $L=1500 \mu H$, $C=18 \mu F$, $n=1.63$ and $K_{IL}=0.030 \Omega$. The other parameters are the same of the 5 kVA inverters.

The experimental results from Fig 9 to Fig 14 are using the first prototype, which has three 5 kVA inverters. Fig 15 shows the results of the prototype with different power inverters. In all tests the maximum load supplied was 10 kVA, because an N+1 redundant structure was designed. Fig 9 shows the voltage output and the inductor currents of the three inverters with a 10 kW resistive load. The currents are balanced, near 17 A RMS in each unit. The inductor currents have a low distortion, which expresses a little power changing among the inverters. This value is low and, in addition, it does not damage the system operation. Besides that, it is minimized by the parallelism control. The output voltage is 216 V RMS, showing the proper static regulation provided by voltage loop controller. Fig 10 shows the same variables for a 10 kVA non-linear load and a 2.5 crest factor. The output voltage has a THD of 4.5% approximately, proving the voltage control strategy by instantaneous average values. The currents are balanced with the inverters 1, 2 and 3 providing 16.3 A RMS, 16.5 A RMS and 17.5 A RMS to the system, respectively. Fig 11 shows the system in non-load operation, which is the worst situation to the parallelism control. The results show that the structure is functioning properly, with no current circulation among inverters. The fundamental components of the currents showed in Fig 11 are in phase and are circulating in the LC filters of the three inverters.

Fig 12 presents the output voltage $V_0$, the currents $I_{L1}$, $I_{L2}$ and $I_{L3}$ during the hot-swap of the inverter 1 in the system under a 10 kVA non-linear load. The voltage does not have expressive transitory, what is typical of damped systems. The currents quickly find a new steady-state operation point. The change in $I_{L1}$ shows the instant of connection of the inverter 1 in the system. Immediately after the connection, the load current is adequately shared among the inverters. The graph of Fig 13 shows the correct division of the load current among the inverters in the whole range of operation. The control strategy presents low THD for $V_0$ voltage with resistive, inductive and non-linear loads, as illustrated in the graphs of Fig 14.

Fig 15 shows the parallel operation of different power inverters. In this test, there are two 5 kVA and one 2.5 kVA inverters connected in parallel supplying a 7.5 kVA non-linear load. With the design of $K_{IL}$ gain 2.5kVA inverter equal to twice $K_{IL}$ gain 5 kVA inverters, the control strategy proposed assures the adequately load current sharing among the parallel inverters, even when these are of different power. Fig 15 shows that 5 kVA inverters currents $I_{L1}$ and $I_{L2}$ are similar, with values of 14.4 A RMS and 14.2 A RMS each. The other current $I_{L4}$ of the 2.5kVA inverter is approximately the half of the others (6.9 A RMS), as it is desirable for this inverter.

The results presented from Fig 9 to Fig 15 prove the efficacy of the parallelism control strategy in the current load sharing among the inverters.
V. CONCLUSION

This paper has proposed a technique for parallel operation of single phase voltage source inverters. Some of the contributions are: the control strategy to the parallelism by instantaneous average values based on the current feedback; and the parallelism control acting in the voltage before the LC filter of each inverter.

Each inverter has its own control system and there is no communication with other inverters. The control in one inverter is composed by two loops: voltage control loop and parallelism control loop. The output voltage control, which is designed using instantaneous average values, ensures a low THD and good static regulation for all kind of loads. The parallelism control is also designed using the same strategy and based on the inductor current feedback. The parallelism control technique showed effective results in the load current sharing in steady-state and transients. The presented results also proved that the presence of the current loop made the system more robust. This fact allowed the connection and disconnection of one inverter in the common AC bus with smooth transitory in $V_0$. It happened due to the damping added...
in the system by the instantaneous inductor current feedback in each inverter.

With parallelism control proposed in this work, the inverters are paralleled without any connection impedance. They work at any level of load, including non-load operation. With this control strategy is also possible to make the parallel operation of different power inverters.

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